forming a semiconductor layer on a substrate;

forming a gate insulating film on said semiconductor layer;

forming a gate electrode above said gate insulating film and a gate line in electrical contact with said gate electrode;

forming a source region and a drain region in said semiconductor layer by adding impurities thereto as donors or acceptors using said gate electrode as a self alignment mask;

simultaneously forming an overlying gate insulator on a top and sidewalls of said gate electrode and said gate line by anodic oxidation of said gate electrode and said gate line to reduce the dimensions of said gate electrode and said gate line and simultaneously form a lateral offset, ΔL, from said source region and said drain region to the sidewalls of said gate electrode; and

forming a data line in electrical contact with said source region and crossing over said gate line at a cross-over location, wherein said overlying gate insulator is located between said data line and said gate line at said cross-over location to insulate said data line from said gate line.

24. The method of claim 23 wherein said gate electrode is comprised of tantalum, and wherein said overlying gate insulator comprises tantalum oxide.

25. The method of claim 23 wherein said gate electrode is selected from the group consisting of tantalum and aluminum.

26. The method of claim 23 wherein the semiconductor layer is a silicon layer formed by decomposing a silane gas using CVD.